Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A capacitor structure comprising:

a substrate;

a first conductive layer disposed on the substrate;

a first insulating layer disposed on the first conductive layer;

a second conductive layer disposed on portions of the first insulating layer;

a second insulating layer disposed on portions of the second conductive layer and the first insulating layer;

a third conductive layer disposed on portions of the second insulating layer and electrically connecting to the first conductive layer through at least one first contact hole, the first contact hole being adjacent to the second conductive layer;

a third insulating layer disposed on the third conductive layer and the second insulating layer; and

a fourth conductive layer disposed on the third insulating layer and electrically connecting to the second conductive layer through at least one second contact hole and a fifth conductive layer, wherein the third conductive layer and the fifth conductive layer are made by a same patterned layer, and the capacitor structure is electrically connected ~~electrically connecting~~ to a thin film transistor (TFT) and the first conductive layer is not electrically connected ~~disconnecting~~ to a gate of the TFT in a display.

Claim 2 (original): The structure of claim 1 wherein the substrate

comprises a glass substrate, a quartz substrate, or a plastic substrate.

Claim 3 (original): The structure of claim 1 wherein the first conductive layer is a polysilicon layer.

Claim 4 (previously presented): The structure of claim 1 wherein the first insulating layer comprises a silicon oxide layer, a silicon nitride layer, or a silicon oxynitride layer.

Claim 5 (original): The structure of claim 1 wherein both of the second conductive layer and the third conductive layer comprise a metal layer, an alloy layer, or a metal multi-layer.

Claim 6 (original): The structure of claim 5 wherein the metal layer comprises a tungsten layer (W layer), a chrome layer (Cr layer), a titanium layer (Ti layer), an aluminum layer (Al layer), a niobium layer (Nb layer), or a molybdenum layer (Mo layer); the alloy layer comprises an aluminum-neodymium (AlNd) alloy, the metal multi-layer comprises a titanium/aluminum/titanium layer (Ti/Al/Ti layer), a molybdenum/aluminum/ molybdenum layer (Mo/Al/Mo layer), or a chrome/aluminum (Cr/Al layer).

Claim 7 (original): The structure of claim 1 wherein the fifth conductive layer is disposed in the second contact hole to electrically connect the fourth conductive layer and the second conductive layer.

Claim 8 (original): The structure of claim 7 wherein the third conductive layer and the fifth conductive layer are not connected.

Claim 9 (previously presented): The structure of claim 7 wherein the substrate is an array substrate of the display, a pixel array area is included on a surface of the substrate, and the fourth conductive layer is

electrically connected to the thin film transistor (TFT) in the pixel array area through the fifth conductive layer.

Claim 10 (original): The structure of claim 9 wherein the capacitor structure is disposed in the pixel array area on the substrate to be used as a storage capacitor.

Claim 11 (previously presented): The structure of claim 1 wherein the substrate is an array substrate of the display, a periphery circuit area is included on a surface of the substrate, and the capacitor structure is disposed in the periphery circuit area on the substrate.

Claim 12 (previously presented): The structure of claim 1 wherein the second insulating layer comprises a silicon oxide layer, a silicon nitride layer, or a silicon oxynitride layer.

Claim 13 (original): The structure of claim 1 wherein the first contact hole is disposed in the first insulating layer and the second insulating layer, and the first contact hole exposes portions of the first conductive layer.

Claim 14 (previously presented): The structure of claim 1 wherein the third insulating layer comprises a silicon oxide layer, a silicon nitride layer, or a silicon oxynitride layer.

Claim 15 (original): The structure of claim 1 wherein the fourth conductive layer comprises an indium tin oxide layer (ITO layer) or an indium zinc oxide layer (IZO layer).

Claim 16 (original): The structure of claim 1 wherein the second contact hole is disposed in the second insulating layer, and the second contact hole exposes portions of the second conductive layer.

Claim 17 (original): The structure of claim 1 wherein the first conductive layer, the first insulating layer, and the second conductive layer form a first capacitor; the second conductive layer, the second insulating layer, and the third conductive layer form a second capacitor; and the third conductive layer, the third insulating layer, and the fourth conductive layer form a third capacitor.

Claim 18 (original): The structure of claim 17 wherein the second conductive layer and the fourth conductive layer are used as a positive electrode of the capacitor, and the second conductive layer and the fourth conductive layer are electrically connected by the fifth conductive layer through the second contact hole; the first conductive layer and the third conductive layer are used as a negative electrode of the capacitor, and the first conductive layer and the third conductive layer are electrically connected through the first contact hole filled with the third conductive layer.

Claim 19 (original): The structure of claim 17 utilizing multi-layered conductive layers as multi-layered electrode plates to form at least two stack capacitors.

Claim 20 (previously presented): The structure of claim 17 wherein the capacitance value of the capacitor is equal to the capacitance value of an equivalent capacitor including the first capacitor, the second capacitor, and the third capacitor connected in parallel with one another.

Claim 21 (previously presented): The structure of claim 9, wherein the gate and the capacitor are in the pixel array area.